FORM PTO-1390 REV. 5-93	US DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTORNEYS DOCKET NUMBER P00,1963
TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371		U.S. APPLICATION NO. (If known, see 37 CFR 1.5) 09/744522
INTERNATIONAL APPLICATION NO. PCT/DE99/02086	INTERNATIONAL FILING DATE 05 JULY 1999	PRIORITY DATE CLAIMED 31 JULY 1998

TITLE OF INVENTION

CIRCUIT AND METHOD FOR CONVERTING DATA IN A PROCESSOR

APPLICANT(S) FOR DO/EO/US

PETER HAAS

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay.
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of International Application as filed (35 U.S.C. 371(c)(2)) - drawings attached.
   a. ☒ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US)
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2) - drawings attached.
7. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
8. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
9. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).
10. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371(c)(5)).

Items 11. to 16. below concern other document(s) or information included:

11. ☒ An Information Disclosure Statement under 37 C.F.R. 1.97 and 1.98; **(PTO 1449, Prior Art, Search Report, References).**
12. ☒ An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. 3.28 and 3.31 is included. **(SEE ATTACHED ENVELOPE)**
13. ☒ Amendment "A" Prior to Action.
    ☐ A SECOND or SUBSEQUENT preliminary amendment.
14. ☒ A substitute specification and substitute specification mark-up.
15. ☒ A change of address letter attached to the Declaration.
16. ☒ Other items or information:
    a. ☒ Submission of Drawings and Drawing Changes
    b. ☒ EXPRESS MAIL #EL655300995US dated January 25, 2001

U.S. APPLICATION NO. (if known, see 37 C.F.R. 1.5) 09/744522	INTERNATIONAL APPLICATION NO. PCT/DE99/02086	ATTORNEY'S DOCKET NUMBER P00,1963

17. ☒ The following fees are submitted:	CALCULATIONS	PTO USE ONLY
BASIC NATIONAL FEE (37 C.F.R. 1.492(a)(1)-(5): Search Report has been prepared by the EPO or JPO . . . . . $860.00 International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) . . $690.00 No international preliminary examination fee paid to USPTO (37 C.F.R. 1.482) but international search fee paid to USPTO (37 C.F.R. 1.445(a)(2) . . . . . $710.00 Neither international preliminary examination fee (37 C.F.R. 1.482) nor international search fee (37 C.F.R. 1.445(a)(2) paid to USPTO . . . . . $1000.00 International preliminary examination fee paid to USPTO (37 C.F.R. 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4) . . . . . $ 100.00		
ENTER APPROPRIATE BASIC FEE AMOUNT =	$ 860.00	
Surcharge of $130.00 for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 C.F.R. 1.492(e)).	$	

Claims	Number Filed	Number Extra	Rate		
Total Claims	11 - 20 =	0	X $ 18.00	$	
Independent Claims	02 - 3 =	0	X $ 80.00	$	
Multiple Dependent Claims			$270.00+	$	
			TOTAL OF ABOVE CALCULATIONS =	$ 860.00	
Reduction by ½ for filing by small entity, if applicable. Verified Small Entity statement must also be filed. (Note 37 C.F.R. 1.9, 1.27, 1.28)				$	
			SUBTOTAL =	$ 860.00	
Processing fee of $130.00 for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492(f)). +				$	
			TOTAL NATIONAL FEE =	$ 860.00	
Fee for recording the enclosed assignment (37 C.F.R. 1.21(h). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. 3.28, 3.31). $40.00 per property +					
			TOTAL FEES ENCLOSED =	$ 860.00	
				Amount to be refunded	$
				charged	$

a. ☒ A check in the amount of $ 860.00 to cover the above fees is enclosed.

b. ☐ Please charge my Deposit Account No. _____ in the amount of $ _____ to cover the above fees. A duplicate copy of this sheet is enclosed.

c. ☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account No. 50-1519. A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 C.F.R. 1.494 or 1.495 has not been met, a petition to revive (37 C.F.R. 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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28,982
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BOX PCT

**IN THE UNITED STATES DESIGNATED/ELECTED OFFICE
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
UNDER THE PATENT COOPERATION TREATY - CHAPTER II**

**AMENDMENT "A" PRIOR TO ACTION AND
SUBMISSION OF SUBSTITUTE SPECIFICATION**

APPLICANTS(S):	HAAS, Peter
ATTORNEY DOCKET NO:	P00,1963
INTERNATIONAL APPLICATION NO:	PCT/DE99/02086
INTERNATIONAL FILING DATE:	05 JUL 1999
INVENTION:	CIRCUIT AND METHOD FOR CONVERTING DATA IN A PROCESSOR

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Applicant herewith submits an amendment and substitute specification in the above-referenced PCT application, and respectfully requests entry of same prior to examination in the United States National Examination Stage.

IN THE SPECIFICATION

Cancel the specification as filed, and insert therefore the substitute specification provided herewith.

IN THE CLAIMS

What is claimed is:

10. A system for data conversion, comprising:

a processor having at least one unit for executing one of a logical or arithmetic operation and an object-oriented data conversion unit for recognizing a type of an object and an object address, the data conversion unit being arranged to precede the unit for executing a logical or arithmetic operation, whereby the data conversion unit recognizes said type of an object based upon a type of information accompanying the object address and matches the type of an object and the object address before one of an operation is performed or a predetermined type of object is generated in the event of non-match.

11. The system according to claim 10, wherein a memory location for the object address and a memory location of a register is respectively divided into a first area and a second area, whereby a type of the object is deposited in the first area.

12. The system according to claim 10, wherein the object-oriented data conversion unit is arranged to follow the unit executing a logical or an arithmetic operation.

13. The system according to claim 10, wherein the object-oriented data conversion unit is arranged to precede the storing of the object in an external storage and a register file.

14. The system according to claim 10, wherein a register file is divided into a memory area for data and a memory area for a respective type indication of the data.

15. The system according to claim 10, further comprising a reduced instruction set processor.

16. The system according to claim 10, further comprising a complex instruction set processor.

17. A method for data conversion in a processor having at least one unit, the method comprising the steps of:

executing a logical or arithmetic operation in the processor;

implementing an object-oriented data conversion by a type information in an object address and by a type information of an object; and

generating an inequality of the objects to be operated by the logical or arithmetic operation based upon the type of objects matched to one another or a predetermined object type of an object.

18. The method according to claim 17, further comprising the steps of:

dividing a memory location for an object address and a memory location of a register into a first and second area and a type information of the memory address deposited in the second area of the object address; and

noting the data of the register deposited in the second area in the first area.

19. The method according to claim 17, wherein the processor includes a reduced instruction set processor.

20. The method according to claim 17, wherein the processor includes a complex instruction set processor.

IN THE ABSTRACT

Cancel the Abstract as filed, and insert therefore on a separate page the following Abstract of the Disclosure:

- - ABSTRACT OF THE DISCLOSURE

A system and method for object-oriented data conversion to be carried out in a processor, before an arithmetic or logical operation is executed, based upon a data type indication belonging to the object. - -

REMARKS

A substitute specification and an Abstract of the Disclosure are provided herewith, which make editorial changes in order to conform to standard US practice. A marked-up copy of the specification is also provided reflecting the changes made.

In addition, the claims as filed have been canceled and replaced by new claims that more clearly set forth the subject matter of Applicant's invention.

No new matter has been inserted into the application.

Applicant submits that this application is in proper condition for examination in the United States National Examination Stage, which action is respectfully requested.

Respectfully submitted,

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Substitute Specification:

- - SYSTEM AND METHOD FOR DATA CONVERSION IN A PROCESSOR

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention belongs to the field of data processors. In particular, the present invention pertains to conversion of data in microprocessors.

Discussion of the Related Art

In processor or microprocessors, the terms will be used interchangeably herein, data conversion is produced by program sequences before arithmetic or logical operations are carried out with different data types. Data type conversion with program sequences has the disadvantage that it reduces the processing speed of a processor or microprocessor. Further, this kind of data type conversion has the disadvantage that the bus system of the processor is additionally loaded by the operation code required for the data type conversion.

In addition to this data type conversion, object-oriented program languages are used to solve specific problems. A data type conversion can also be achieved by an object-oriented command structure. However, object-oriented command structure has the disadvantage that each command for each combination of data types must be deposited in the memory. An enlargement of the program code likewise results in a reduction of the processing speed.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a reliable and efficient system and method for data type conversion.

It is another object of the present invention to provide a system and method for data conversion can be implemented without reducing the processing speed of the processor.

It is a further object of the invention to provide a system and method for data conversion wherein data type conversions are automatically implemented.

It is an additional object of the invention to provide a system and method for data conversion wherein the program code used need not be enlarged.

It is yet another object of the invention to provide a system and method for data conversion wherein a data type-suited data type conversion is implemented with a data type-suited address calculation.

BRIEF DESCRIPTION OF THE DRAWING FIGURES

Figure 1 shows the structure of an object address according to the present invention;

Figure 2 shows the structure of a register according to the present invention;

Figure 3 shows the structure of internal registers according to the present invention;

Figure 4 shows an embodiment of a processor according to the present invention; and

Figure 5 shows the embodiment of the processor with an object-oriented data type conversion according to the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Figure 1 shows a division of an object address OA. This object address OA is divided into an area for the specification of the type T of object and a memory address SA belonging to the object. The memory address SA indicates the memory location of an object in a memory area of a memory. The object type T and the memory address SA are assigned by a compiler given a declaration of the object and are treated as a unit. For example, objects can be data, addresses or code addresses.

Figure 2 shows the division of a register R. This register R is divided into a first area for indicating the data or, respectively, object type T and into a second area for storing the data or, respectively, objects D.

Figure 3 shows a detailed specification of the division of the register R and of the object address OA. In this illustration, the addresses or data to be stored are divided into a first and second area, as indicated above. For example, 3 bits for the indication of the object type T and 32 bits for the object to be stored, the address or data are provided in a register R having a length of 35 bits. The 32 bits for the object can be a data word, a data or code address or a memory address with a particular about the type of memory address. Further subdivisions are shown in Figure 3.

Figure 4 shows a processor, particularly an RISC (reduced instruction set code) processor. In this illustration, the critical components of the RISC processor arranged in a pipeline are a sequence controller SC, an instruction decode ID, a

register read unit RR, an execute unit E, a data transfer unit DT and a register write unit RW. Data are either read in or out from an external storage unit M via the data transfer unit DT. Data that are of significance for the ongoing processing process are deposited in a register file RF via the register write unit RW and are in turn read as needed by the data read unit RR. Logical and arithmetic instructions are executed in the execute unit E.

In Figure 5, the RISC processor is formed with at least one data type conversion unit TC that carries out a data type conversion. This data type conversion unit can be arranged before and after the execute unit E or between the external storage unit M and the data transfer unit DT. The data type conversion unit can likewise be arranged between the register write unit RW and the register file RF and between the register file RF, and the register read unit RR in order to implement a data conversion that becomes necessary. As shown in Figure 5, a data type conversion unit TC in the data pipeline of the RISC processor that the clock frequency of the pipeline remains unmodified.

In the present invention, the object address OA is divided into a first and second area. The data type conversion unit T^C determines the data type T from the first area and the physical address SA from the second area.

Given a memory access, an address calculation of indicated load and store instructions is made with the assistance of the object type, before an address offset corresponding to the object size is determined for the physical address SA.

Given a load instruction, the memory address of the object is known. The object is deposited in a register of the processor with the indication of the type.

Given a store instruction, the data to be stored and the object type pertaining thereto are taken from the register, converted into the object type of the destination address and deposited under the destination address.

In addition to containing the register numbers of source and destination registers, execute instructions also contain the object type for the destination register. The object type of the operation is derived from the object type of the destination register. A processing unit in the execute unit E, such as an arithmetic operation, is selected on the basis of the object type. Since the object types of the source and destination registers are known before an arithmetic operation, a data type conversion can be undertaken. Before an operation, the source data are converted into a data type that can be processed by an execute unit E of an RISC processor. After an operation, the result can be converted into the data type of a destination register.

Given a multiplication of a first and second variable, the compiler generates the physical address and the data type. When loading the first and second variable, the data types are deposited in the register file RF. The program section – load variable 1 – signals the size of the first variable to the processor, for example an 8 bit value or 16 bit value. With the data type, the data type conversion unit TC is informed whether it is a matter of a signed integer variable, or of an unsigned integer variable. After the loading of the first variable, the data belonging to the second variable are loaded. Since, upon reading the data from the register file RF, the data type conversion unit TC knows the two data types of the first and second variable, the data types are adapted to one another and the actual operation such as, for example, a multiplication is executed in the following execute unit E.

The data type conversion unit TC can be introduced into the data pipeline of the RISC processor at various locations following the execute unit E. A lack of the data type conversion unit TC following the execute unit E results, such that the result data formed in the execute unit E are deposited in the register file RF together with a data type deriving from the respective operation.

Given a store instruction, both the data as well as the respective data type are again read from the register file RF and supplied to a data type conversion unit TC preceding the execute unit E. The data type conversion according to the data type of the destination address follows from there.

Given an indexed addressing, the data type conversion unit TC need only be informed of the simple index, and the processor can calculate the byte offset on the basis of the data type of the address. Given a normal integer value that exhibits a length of 2 bytes for example, it is thus known that the index must be correspondingly doubled and added to the physical address. This has the advantage that time-consuming conversions for determining the address indices are eliminated.

An advantage of the indexed address calculation is based upon the fact that a table of data with short integer values, long integer values or normal integer values can be processed with one and the same program code. Therefore, the program code need not distinguish between the data types, since the processor calculates its addresses itself on the basis of the data types.

As an alternative to using a RISC processor, the present invention can be implemented using a CISC (complex instruction set code) processor in the same manner as described above for the RISC processor.

Although preferred embodiments of the invention have been described herein, it is to be understood that the invention is not limited to these embodiments, but that various changes and modifications thereto may be made by persons having skill in the art to which this invention pertains, without departing from the scope and spirit of the invention, which is to be defined by the following claims. - -

Siemens AG
New PCT application
26965-0726 (P-00,1968)
1998 P 02216 WO US
Inventor: Haas

Translation / January 11, 2001 / 1696(911) / 2040 words

CIRCUIT ARRANGEMENT AND METHOD FOR DATA CONVERSION IN A PROCESSOR

In processor or microprocessors, a data conversion is produced by program sequences before arithmetic or logical operations with different data types. Data type conversion with program sequences, however, has the disadvantage that it reduces the processing speed of a processor or microprocessor. Further, this kind of data type conversion exhibits the disadvantage that the bus system of the processor is additionally loaded by the operation code required for the data type conversion.

In addition to the data type conversion that has been mentioned, object-oriented program languages are utilized in order to solve specific problems. A data type conversion can also be achieved by an object-oriented command structure. The object-oriented command structure, however, produces the disadvantage that each command for each combination of data types must be deposited in the memory. An enlargement of the program code likewise results in a reduction of the processing speed.

The invention is based on the object of specifying a circuit arrangement and a method for data type conversion that avoids the aforementioned disadvantages.

This object is achieved by the features of patent claim 1 and 8.

The invention yields the advantage that a data conversion can be implemented without reducing the processing speed of the processor.

The invention yields the advantage that data type conversions are automatically implemented.

The invention yields the further advantage that the program code need not be enlarged.

The invention yields the further advantage that a data type-suited data type conversion is implemented with a data type-suited address calculation.

Further characteristics are recited in the subclaims.

The circuit arrangement and the method can be seen from the following, more detailed explanation of an exemplary embodiment with reference to drawings.

Shown are:

Figure 1 the structure of an object address;

Figure 2 the structure of a register;

Figure 3 the structure of internal registers;

Figure 4 an embodiment of a processor; and

Figure 5 the embodiment of the processor with an object-oriented data type conversion according to the invention.

Figure 1 shows a division of an object address OA. This object address OA is divided into an area for the specification of the type T of object and a memory address SA belonging to the object. The memory address SA indicates the memory location of an object in a memory area of a memory. The object type T and the memory address SA are assigned by a compiler given a declaration of the object and are treated as a unit. For example, objects can be data, addresses or code addresses.

Figure 2 shows the division of a register R. This register R is divided into a first area for indicating the data or, respectively, object type T and into a second area for storing the data or, respectively, objects D.

Figure s shows a detailed specification of the division of the register R and of the object address OA. In this illustration, the addresses or data to be stored are divided into a first and second area, as indicated above. For example, 3 bits for the indication of the object type T and 32 bits for the object to be stored, the address or data are provided in a register R having a length of 35 bits. The 32 bits for the object can be a data word, a data or code address or a memory address with a particular about the type of memory address. Further subdivisions are shown in Figure 3.

Figure 4 shows a processor, particularly an RISC processor. In this illustration, the critical components of the RSIC processor arranged in a pipeline are a sequence controller SC, an instruction decode ID, a register read unit RR, an execute unit E, a data transfer unit DT and a register write unit RW. Data are either read in or out from an external storage unit M via the data transfer unit DT. Data that are of significance for the ongoing processing process are deposited in a register file RF via the register write unit RW and are in turn read as needed by the data read unit RR. Logical and arithmetic instructions are executed in the execute unit E.

In Figure 5, the RISC processor is fashioned with at least one data type conversion unit TC that implements a data type conversion. This data type conversion unit can, for example, be arranged before and after the execute unit E or between the external storage unit M and the data transfer unit DT. The data type conversion unit can likewise be arranged between the register write unit RW and the register file RF and between the register file RF and the register read unit RR in order to implement a data conversion that becomes necessary. The illustrated arrangement with a data type conversion unit TC in the data pipeline of the RISC processor yields the advantage that the clock frequency of the pipeline remains unmodified.

In the present invention, the object address OA is divided into a first and second area. The data type conversion unit T^C determines the data type T from the first area and the physical address SA from the second area.

Given a memory access, an address calculation of indicated load and store instructions [...] with the assistance of the object type [...] an address offset corresponding to the object size is determined for the physical address SA.

Given a load instruction, the memory address of the object is known. The object is deposited in a register of the processor with the indication of the type.

Given a store instruction, the data to be stored and the object type appertaining thereto are taken from the register, converted into the object type of the destination address and deposited under the destination address.

In addition to containing the register numbers of source and destination registers, execute instructions also contain the appertaining object type for the destination register. The object type of the operation is derived from the object type of the destination register. A processing unit in the execute unit E for, for example, an arithmetic operation is selected on the basis of the object type. Since the object types of the source and destination registers are known before an arithmetic operation, a data type conversion can be correspondingly undertaken. Before an operation, the source data are converted into a data type that can be processed by an execute unit E of an RISC processor. After an operation, the result can be converted into the data type of a destination register.

Given a multiplication of a first and second variable, the compiler respectively generates the physical address and the data type. When loading the first and second variable, the data types are deposited in the register file RF. The program section – load variable 1 – signals the size of the first variable to the processor, for example an 8 bit value or 16 bit value. With the data type, the data type conversion unit TC is informed whether it is a matter of a signed integer variable or of an unsigned integer variable. After the loading of the first variable, the data belonging to the second variable are loaded. Since, upon reading the data from the register file RF, the data type conversion unit TC knows the two data types of the first and second variable, the data types are adapted to one another and the actual operation such as, for example, a multiplication is executed in the following execute unit E.

The data type conversion unit TC can be introduced into the data pipeline of the RISC processor at various locations following the execute unit E. A lack of the data type conversion unit TC following the execute unit E results therein that the result data that were formed in the execute unit E are deposited in the register file RF together with a data type deriving from the respective operation.

Given a store instruction, both the data as well as the respective data type are again read from the register file RF and supplied to a data type conversion unit TC preceding the execute unit E. The data type conversion according to the data type of the destination address can ensue there.

Given an indexed addressing, the data type conversion unit TC need only be informed of the simple index, and the processor can calculate the byte offset on the basis of the data type of the address. Given a normal integer value that exhibits a length of 2 bytes, for example, it is thus known that the index must be correspondingly doubled and added to the physical address therefor. This yields the advantage that time-consuming conversions for determining the address indices are eliminated.

Another advantage of the indexed address calculation is comprised therein that a table of data with short integer values or long integer values or normal integer values can be processed with one and the same program code. The program code

thereby need not distinguish between said data types since the processor calculates its addresses itself on the basis of the data types.

Patent Claims

1. Circuit arrangement for data conversion in a processor having at least one unit (E) executing a logical or arithmetic operation, characterized in that an object-oriented data conversion unit (TC) for recognizing a type (T) of an object (D) and an object address (OA) is arranged preceding the unit (E) executing the logical or arithmetic operation, and, based on the type information accompanying an object address (OA) and the object (D), the data conversion unit (TC) recognizes the type (T) of the object (D) and, given non-uniformity, matches the objects (D) before an operation or generates a predetermined type of object (D).

2. Circuit arrangement according to claim 1, characterized in that a memory location for an object address (OA) and a memory location of a register (R) is respectively divided into a first and second area (T, SA; T, D), whereby a type (T) of the object (SA, D) is respectively deposited in the first area.

3. Circuit arrangement according to claim 1, characterized in that the object-oriented data conversion unit (TC) is provided following the unit (E) executing a logical or an arithmetic operation.

4. Circuit arrangement according to claim 1, characterized in that the object-oriented data conversion unit (TC) is arranged preceding the storing of the object (D) in an external storage (M) and a register file (RC).

5. Circuit arrangement according to claim 1, characterized in that a register file (RC) is divided into a memory area for data and a memory area for a respective type indication of the data.

6. Circuit arrangement according to claim 1, characterized in that this is a reduced instruction set computer (RISC).

7. Circuit arrangement according to claim 1, characterized in that this is a complex instruction set computer (CISC).

8. Method for data conversion in a processor having at least one unit (E) executing a logical or arithmetic operation, characterized in that an object-oriented data conversion is implemented by a type information (T) in an object address (OA) and by a type information (T) of an object (D), and, given an inequality of the objects

(D) to be operated by a logical or arithmetic operation, the type of the objects is matched to one another or a predetermined object type of an object (D) is generated.

9. Method according to claim 8, characterized in that a memory location for an object address (OA) and a memory location of a register (R) is respectively divided into a first and second area (T, SA; T, D), and a type information of the memory address (SA) deposited in the second area of the object address (OA) and the data (D) of the register (R) deposited in the second area is respectively noted in the first area (T).

Abstract

Circuit Arrangement and Method for Data Conversion in a Processor

A data conversion to be implemented in a processor is implemented object-oriented before an arithmetic or logical operation, being respectively implemented on the basis of a data type indication belonging to the object.

Figure 3

FIG 1

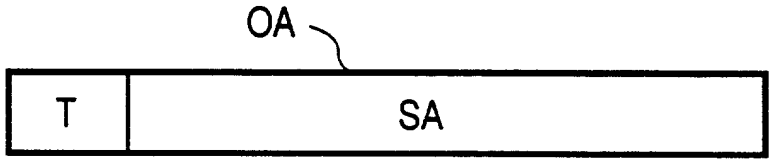


FIG 2

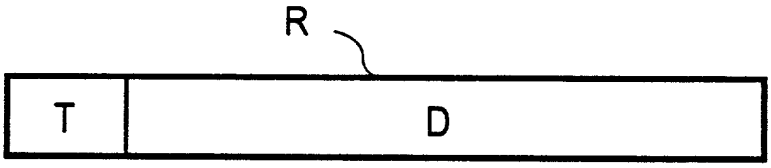


FIG 3

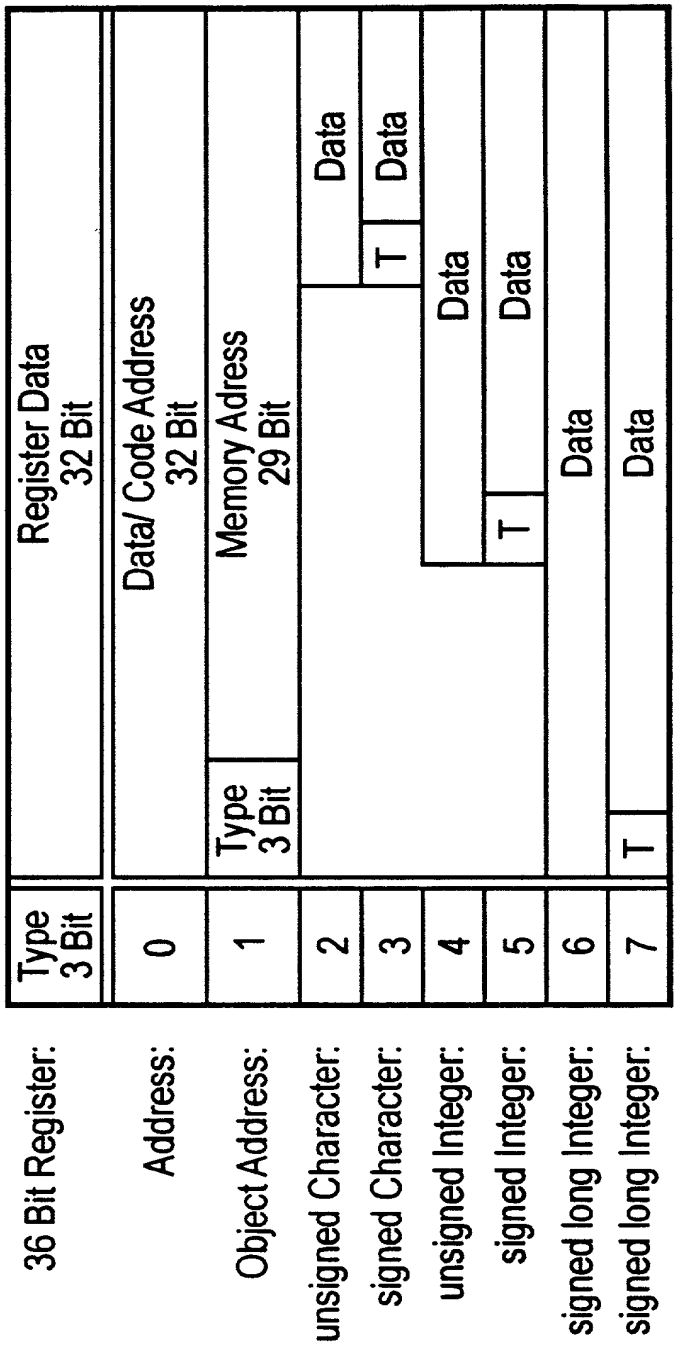

36 Bit Register:
Address:
Object Address:
unsigned Character:
signed Character:
unsigned Integer:
signed Integer:
signed long Integer:
signed long Integer:
Type 3 Bit
Register Data 32 Bit
Data/ Code Address 32 Bit
Type 3 Bit
Memory Adress 29 Bit
0
1
2
3
4
5
6
7
Data
T
Data
T
Data
T
Data
T
Data

FIG 4

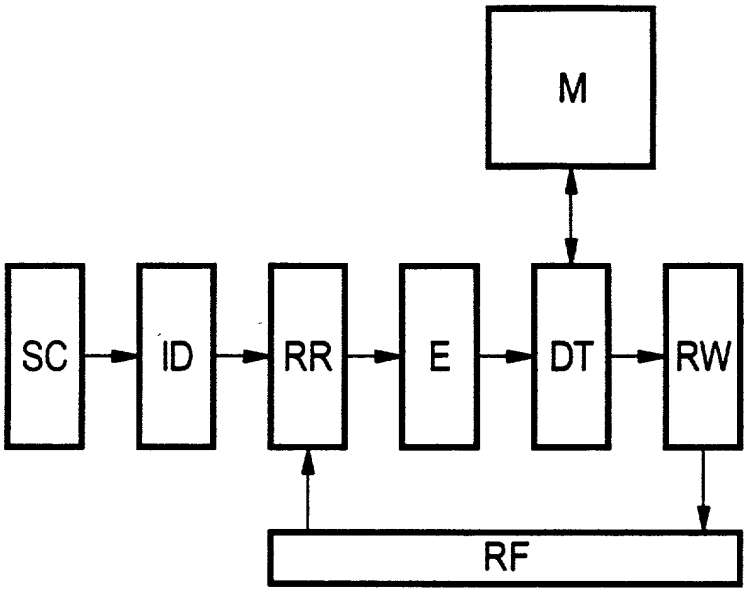
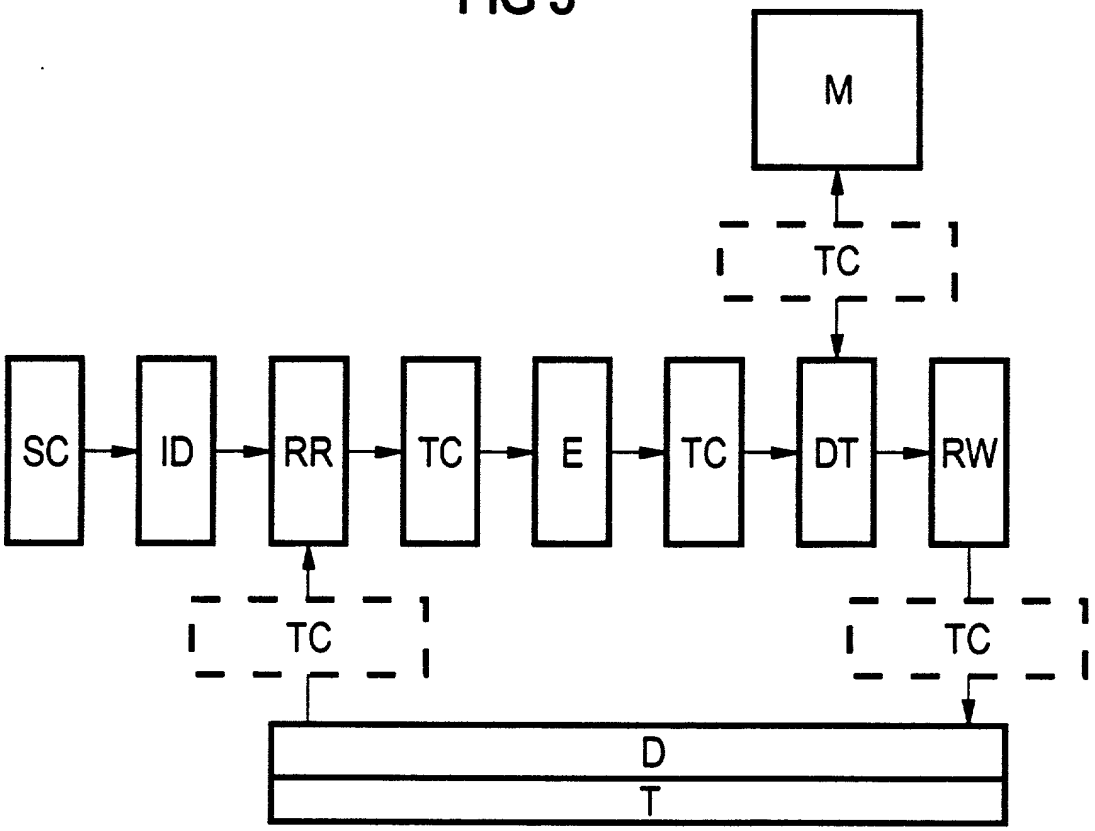


FIG 5



Declaration and Power of Attorney For Patent Application
Erklärung Für Patentanmeldungen Mit Vollmacht
German Language Declaration

Als nachstehend benannter Erfinder erkläre ich hiermit an Eides Statt:

As a below named inventor, I hereby declare that:

dass mein Wohnsitz, meine Postanschrift, und meine Staatsangehörigkeit den im Nachstehenden nach meinem Namen aufgeführten Angaben entsprechen,

My residence, post office address and citizenship are as stated below next to my name,

dass ich, nach bestem Wissen der ursprüngliche, erste und alleinige Erfinder (falls nachstehend nur ein Name angegeben ist) oder ein ursprünglicher, erster und Miterfinder (falls nachstehend mehrere Namen aufgeführt sind) des Gegenstandes bin, für den dieser Antrag gestellt wird und für den ein Patent beantragt wird für die Erfindung mit dem Titel:

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

<u>Schaltungsanordnung und Verfahren zur Datenkonvertierung in einem Prozessor</u>

deren Beschreibung

the specification of which

(zutreffendes ankreuzen)

- [x] hier beigefügt ist.
- [ ] am ____________ als PCT internationale Anmeldung PCT Anmeldungsnummer ____________ eingereicht wurde und am ____________ abgeändert wurde (falls tatsächlich abgeändert).

(check one)

- [x] is attached hereto.
- [ ] was filed on ____________ as PCT international application PCT Application No. ____________ and was amended on ____________ (if applicable)

Ich bestätige hiermit, dass ich den Inhalt der obigen Patentanmeldung einschliesslich der Ansprüche durchgesehen und verstanden habe, die eventuell durch einen Zusatzantrag wie oben erwähnt abgeändert wurde.

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims as amended by any amendment referred to above.

Ich erkenne meine Pflicht zur Offenbarung irgendwelcher Informationen, die für die Prüfung der vorliegenden Anmeldung in Einklang mit Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) von Wichtigkeit sind, an.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56(a).

Ich beanspruche hiermit ausländische Prioritätsvorteile gemäss Abschnitt 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 119 aller unten angegebenen Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde, und habe auch alle Auslandsanmeldungen für ein Patent oder eine Erfindersurkunde nachstehend gekennzeichnet, die ein Anmeldedatum haben, das vor dem Anmeldedatum der Anmeldung liegt, für die Priorität beansprucht wird.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

German Language Declaration

Prior foreign appplications
Priorität beansprucht

			Priority Claimed	
19834632.8	Germany	31. July 1998	☒ Yes / Ja	☐ No / Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)		
			☐ Yes / Ja	☐ No / Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)		
			☐ Yes / Ja	☐ No / Nein
(Number) (Nummer)	(Country) (Land)	(Day Month Year Filed) (Tag Monat Jahr eingereicht)		

Ich beanspruche hiermit gemäss Absatz 35 der Zivilprozessordnung der Vereinigten Staaten, Paragraph 120, den Vorzug aller unten aufgeführten Anmeldungen und falls der Gegenstand aus jedem Anspruch dieser Anmeldung nicht in einer früheren amerikanischen Patentanmeldung laut dem ersten Paragraphen des Absatzes 35 der Zivilprozeßordnung der Vereinigten Staaten, Paragraph 122 offenbart ist, erkenne ich gemäss Absatz 37, Bundesgesetzbuch, Paragraph 1.56(a) meine Pflicht zur Offenbarung von Informationen an, die zwischen dem Anmeldedatum der früheren Anmeldung und dem nationalen oder PCT internationalen Anmeldedatum dieser Anmeldung bekannt geworden sind.

I hereby claim the benefit under Title 35. United States Code. §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §122, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occured between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgegeben)	(Status) (patented, pending, abandoned)
(Application Serial No.) (Anmeldeseriennummer)	(Filing Date) (Anmeldedatum)	(Status) (patentiert, anhängig, aufgeben)	(Status) (patented, pending, abandoned)

Ich erklare hiermit, dass alle von mir in der vorliegenden Erklärung gemachten Angaben nach meinem besten Wissen und Gewissen der vollen Wahrheit entsprechen, und dass ich diese eidesstattliche Erklärung in Kenntnis dessen abgebe, dass wissentlich und vorsätzlich falsche Angaben gemäss Paragraph 1001, Absatz 18 der Zivilprozessordnung der Vereinigten Staaten von Amerika mit Geldstrafe belegt und/oder Gefangnis bestraft werden koennen, und dass derartig wissentlich und vorsätzlich falsche Angaben die Gültigkeit der vorliegenden Patentanmeldung oder eines darauf erteilten Patentes gefährden können.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon

German Language Declaration

VERTRETUNGSVOLLMACHT: Als benannter Erfinder beauftrage ich hiermit den nachstehend benannten Patentanwalt (oder die nachstehend benannten Patentanwälte) und/oder Patent-Agenten mit der Verfolgung der vorliegenden Patentanmeldung sowie mit der Abwicklung aller damit verbundenen Geschäfte vor dem Patent- und Warenzeichenamt: *(Name und Registrationsnummer anführen)*

POWER OF ATTORNEY. As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

And I hereby appoint

Messrs. John D. Simpson (Registration No. 19,842) Lewis T. Steadman (17,074), William C. Stueber (16,453), P. Phillips Connor (19,259), Dennis A. Gross (24,410), Marvin Moody (16,549), Steven H. Noll (28,982), Brett A. Valiquet (27,841), Thomas I. Ross (29,275), Kevin W. Guynn (29,927), Edward A. Lehmann (22,312), James D. Hobart (24,149), Robert M. Barrett (30,142), James Van Santen (16,584), J. Arthur Gross (13,615), Richard J. Schwarz (13,472) and Melvin A. Robinson (31,870), David R. Metzger (32,919), John R. Garrett (27,888) all members of the firm of Hill, Steadman & Simpson, A Professional Corporation.

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Voller Name des einzigen oder ursprünglichen Erfinders: HAAS, Peter	Full name of sole or first inventor:
Unterschrift des Erfinders Datum 12. Juli 99	Inventor's signature Date
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Postanschrift Dr.-Hartlaub-Ring 25/V	Post Office Addess
D-85570 Markt Schwaben Bundesrepublik Deutschland	
Voller Name des zweiten Miterfinders (falls zutreffend):	Full name of second joint inventor, if any:
Unterschrift des Erfinders Datum	Second Inventor's signature Date
Wohnsitz	Residence
Staatsangehörigkeit	Citizenship
Postanschrift	Post Office Address

(Bitte entsprechende Informationen und Unterschriften im Falle von dritten und weiteren Miterfindern angeben).

(Supply similar information and signature for third and subsequent joint inventors).